

IN THE CLAIMS

1-32. (Canceled)

33. (Canceled)

34. (Currently Amended) The vertical transistor according to claim 35 ~~33~~, wherein the electrode has an electrode upper surface that is below the substrate upper surface.

35. (Currently Amended) ~~The A~~ vertical transistor, comprising: according to claim 33,
~~further including:~~

a semiconductor substrate comprising an upper surface;

a recess disposed in the upper surface, wherein the recess contains a localized epitaxial semiconductor film comprising more than three monolithic surfaces;

a gate dielectric layer disposed over the localized epitaxial semiconductor film;

an electrode disposed in the recess over the gate dielectric layer; and

a silicon-deuterium transition layer, or a silicon-hydrogen transition layer, or a silicon-hydrogen-deuterium transition layer disposed between the more than three monolithic surfaces and the gate dielectric layer.

36. (Currently Amended) The vertical transistor according to claim 35 ~~33~~, wherein the gate dielectric layer is selected from a refractory metal oxide, a thermal oxide, a silicon oxide, a silicon oxynitride, a silicon nitride, a carbon-doped oxide, and combinations thereof.

37. (Currently Amended) The vertical transistor according to claim 35 ~~33~~, wherein the electrode is doped polysilicon.

38. (Currently Amended) The vertical transistor according to claim 35 ~~33~~, wherein the substrate includes:

an N+ doped source and an N+ doped drain disposed on opposite sides of the recess.

39. (Currently Amended) The vertical transistor according to claim ~~35~~ 33, wherein the substrate includes:

an N+ doped source and an N+ doped drain disposed on opposite sides of the recess; and
wherein the source and drain are bounded in a first dimension by a structure having a minimum photolithographic feature.

40. (Currently Amended) The vertical transistor according to claim ~~35~~ 33, wherein the substrate includes:

an N+ doped source and an N+ doped drain disposed on opposite sides of the recess;
wherein the source and drain are bounded in a first dimension by a first STI structure having a first minimum photolithographic feature; and
wherein the source and ~~or~~ the drain ~~is~~ are bounded in a second dimension by a second STI structure having a second minimum feature dimension that is substantially equal to the first minimum feature dimension.

41. (Currently Amended) The vertical transistor according to claim ~~35~~ 33, wherein the substrate includes:

an N+ doped source and an N+ doped drain disposed on opposite sides of the recess;
wherein the source and drain are bounded by a first STI structure;
wherein the source and ~~or~~ the drain ~~is~~ are bounded by a second STI structure;
wherein the recess is disposed in the substrate to a first depth; and
wherein the STI structures are disposed in the substrate to a second depth, and wherein the second depth is greater than the first depth.

42. (Currently Amended) ~~The~~ A vertical transistor, comprising: according to claim 33,
a semiconductor substrate comprising an upper surface;
a recess disposed in the upper surface, wherein the recess contains a localized epitaxial
semiconductor film comprising more than three monolithic surfaces;
a gate dielectric layer disposed over the localized epitaxial semiconductor film;

an electrode disposed in the recess over the gate dielectric layer; and

wherein substrate includes:

an N+ doped source and an N+ doped drain disposed on opposite sides of the recess;
wherein the N+ doped source and the N+ doped drain are bounded in a first dimension by
a first STI structure;
wherein the N+ doped source and the N+ doped drain are bounded in a second dimension
by a second STI structure; and
wherein the STI structures are each disposed within a recess including a curvilinear
epitaxial film.

43. (Canceled)

44. (Currently Amended) The electrical device according to claim 45 43, wherein the
electrode has an electrode upper surface that is below the substrate upper surface.

45. (Currently Amended) ~~The~~ An electrical device ~~according to claim 43, further including~~
comprising:

a substrate comprising an upper surface;
an active area disposed in the substrate comprising a source and a drain;
a recess disposed between the source and the drain, wherein the recess comprises a
substantially curvilinear bottom profile of epitaxial semiconductive material;
a gate dielectric layer disposed over the epitaxial semiconductive material;
an electrode disposed over the gate dielectric layer; and
a silicon-deuterium transition layer, or a silicon-hydrogen transition layer, or a silicon-
hydrogen-deuterium transition layer disposed between the substantially curvilinear bottom
profile of epitaxial semiconductive material and the gate dielectric layer.

46. (Currently Amended) The electrical device according to claim 45 43, wherein the gate
dielectric layer is selected from a refractory metal oxide, a thermal oxide, a silicon oxide, a
silicon oxynitride, a silicon nitride, a carbon-doped oxide, and combinations thereof.

47. (Currently Amended) The electrical device according to claim 45 43, wherein the electrode is doped polysilicon.

48. (Currently Amended) The electrical device according to claim 45 43, wherein the substrate includes:

an N+ doped source and an N+ doped drain disposed on opposite sides of the recess; and
wherein the source and drain are bounded in a first dimension by a first shallow trench isolation structure comprising a minimum photolithographic feature.

49. (Currently Amended) The electrical device according to claim 45 43, wherein the substrate includes:

an N+ doped source and an N+ doped drain disposed on opposite sides of the recess;
wherein the source and drain are bounded in a first dimension by a first shallow trench isolation structure comprising a minimum photolithographic feature; and
wherein the source and the drain are bounded in a second dimension by a second shallow trench isolation structure including the minimum photolithographic feature.

50-55. (Canceled)

56. (Currently Amended) An electrical device comprising:

a semiconductor substrate including an upper surface;
a recess disposed in the upper surface wherein the recess exhibits ~~is covered with~~ a substantially curvilinear bottom profile including epitaxial semiconductive material;
a first gate dielectric layer disposed over the epitaxial semiconductive material;
a floating gate film disposed over the first gate dielectric layer;
a second gate dielectric layer disposed over the floating gate film; and
an electrode disposed over the second gate dielectric layer.

57. (Original) The electrical device according to claim 56, further including:
a first shallow trench isolation (STI) structure disposed immediately adjacent the recess.
58. (Original) The electrical device according to claim 56, further including:
a first shallow trench isolation (STI) structure disposed immediately adjacent the recess;
and
a second STI structure disposed in the semiconductor substrate in a direction parallel to the first STI.
59. (Original) The electrical device according to claim 56, further including:
a chip package, wherein the semiconductor substrate is disposed in the chip package; and
a host, wherein the chip package is disposed in the host.
60. (Original) The electrical device according to claim 56, further including:
a chip package, wherein the monocrystalline semiconductor substrate is disposed in the chip package;
a host, wherein the chip package is disposed in the host, wherein the host comprises a chip set; and
an electronic system, wherein the chip set is disposed in the electronic system.
- 61-62. (Canceled)